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EXAMINER	
BASIAGA, DARIUSZ	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,353	LEE, DOUGLAS C.	
	Examiner	Art Unit	
	Dariusz K. Basiaga	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1,2,7,13,17,18 and 21 are rejected the words/phrase "would have been" and "if" renders the claim indefinite. The examiner questions the meets and bounds of the claim for what would the claim represent if the eventuality arises of a "would not have been" or "if not". Therefore, the description of the invention following "would have been" and "if" in the claim is being considered in the rejection but it does not play a crucial part in the consideration as the statutory determinant of the prior art.

Regarding claims 1,2,7,13,17,18 and 21, the phrase "closely mimic" renders the claim indefinite because the meets and bounds of the claim are unclear. The examiner questions how close is close?

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

1. Claims 1-29 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 1-29 are directed to a program, per se, not stored on computer-readable medium in an executable format so as to enable a computer to execute a practical application with a useful, concrete and tangible result.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claim 1-4,6,7,9,10,13,15-21,24,27 and 28 rejected under 35 U.S.C. 103(a) as being unpatentable over ***A tool for the Design and Evaluation of Fiber Channel Storage Area Networks*** by Xavier Molero et al. here in "Molero", and U.S. Patent 6,112,278 titled ***Method to Store Initiator Information for SCSI Data Transfer*** by Jackson L. Ellis herein "Ellis".

As per claim 1, Molero teaches **a software-implemented shared bus system model for modeling a shared bus system that includes a plurality of devices interconnected via a shared bus**. Molero employs a CSIM language as the software to be used in simulating the system (Molero Page 135, left column near bottom), the software creates a "server" processes (plurality of devices) which connects to the Storage Area Network (SAN) / BUS. (Molero, Page 135, right column near the center) Also Molero teaches a ***first device model for partially modeling a first one of said plurality of devices, said first device model including a first modified logical module and a first modified I/O-specific module.*** Molero models a server/storage device (1st of plurality of devices) which capable of generating I/O operations (I/O-specific module) and data messages/packets (logical module). (Molero, Page 135, Left column Center).

Molero does not explicitly teach a **sharable module having provisioned therein first shareable data, said first shareable data being shareable by said first device model and another device model of said plurality of device models, said first shareable data representing I/O-specific data associated with said first device model that is also needed by said another device model of said plurality of device models during configuration of said shared bus system model, said first shareable data further representing data that would have been provisioned within said first device model if said first device model had been configured to closely mimic the data content of**

said first one of said plurality of devices, said first shareable data instead of being provisioned in said shareable module. Although, Molero does state modeling a device (server) that contains the ability to generate I/O specific data. The I/O specific data and the method at which it's being created and transmitted is designed to mirror (mimic) the way a physical device (server) would have handled the data (Molero, Page 135, Right Column near center). Still, Molero does not mention that the system contains a shareable module having provisioned I/O specific shareable data. However, Ellis mentions a method of having ***several initiators with the same parameters, support for all initiators (devices) is provided by storing sets of parameters (I/O data) and corresponding lists of initiator ID's in cache entries (part of shareable module). Based on the initiator ID in a selection command, the target selects the appropriate parameters and automatically transitions to data transfer.***(Ellis, Column 3, Lines 16-23) Also Ellis mentions that the stored parameters consist of period, offset, wide/narrow and speed which as can be seen define a set of I/O-specific data parameters that allow for configuration of the bus system. (Ellis, Column 4, Lines 54-56) It would have been obvious to one of ordinary skill in the art to combine the teachings of Molero with the teachings of Ellis. By combining the teachings one would be able to simulate larger device bus structures without increasing the architectural and processing overhead. (Ellis, Column 3, Lines 12 and 13).

Limitations of claim 2 are rejected for the same reasons outlined in rejection of claim 1. Also it can be seen that both Molero and Ellis teach a method of bus simulation with multiple of devices. (Molero Page 133, left Column Near top, Page 135, Left column Center, Ellis, Column 3 Lines 15-25)

As per claim 3, Molero does not teach that ***the software-implemented shared bus system model of claim 2 wherein said shared bus represents a SCSI (Small Computer System Interface) bus.*** However, Ellis teaches that the bus configuration depicted in the example is a SCSI bus. (Ellis, Column 4, Lines 23 and 24). It would have been obvious to one of ordinary skill to combine the teachings of Molero with Ellis in order to employ the bus device simulation method beyond a SAN bus configuration into SCSI bus configuration. As a result one would be able to test a great variety of devices while still benefiting of the reduced system overhead thought by Ellis.

As per claim 4, Molero teaches a **the software-implemented shared bus system model of claim 2 wherein said first shareable data includes timing information specific to said first one of said plurality of devices.** Molero states that one of the input parameters for the I/O traffic ***contain(s) information about the time when the I/O request starts.***(Molero, Page 138, near center) Molero also states that another important input parameter is ***propagation time delay along the physical link (measured in clock cycles) and link bandwidth (measured in bytes per clock cycle).***(Molero, Page 138, near top) An

ordinarily skilled artisan would find it obvious that the information about the time of the I/O and the propagation time delay of the data is the timing information specific to one of the mentioned devices.

As per claim 6, Molero does not teach that **the software-implemented shared bus system model of claim 2 wherein said shareable module further includes a protocol monitor module, said protocol monitor module having access to said first shareable data and said second shareable data to configure, during configuration of said shared bus system model, said protocol monitor module to facilitate monitoring of interactions at the protocol level, during execution, among said first device model, said second device model, and said timing monitor module.** However Ellis teaches a ***protocol engine (ACS) connected to the SCSI bus. ACS is a master state machine providing the requisite automated logic for sequencing through the SCSI phases and receiving initiator requests. Cache entries may be selected by ACS...*** (Ellis, Column 4, Lines 44-48) ***Each cache entry contains a set of initiator parameters, such as period, offset, wide/narrow, and speed. In addition to initiator parameters each cache entry also contains a plurality of bits corresponding to the initiators which may be supported by the parameters in that cache entry.*** (Ellis, Column 4, Lines 54-59). An ordinarily skilled artisan would find it obvious that the protocol engine (ACS) described by Ellis is functionally equivalent to the protocol engine described by the applicant.

As per claim 7, Molero does not teach **that the software-implemented shared bus system model of claim 2 wherein said shareable module further includes shareable logic, said shareable logic representing logic functions executable on behalf of said first device model and said second device model, said shareable logic further representing a logic function that would have been provisioned within each of said first device model and said second device model if said first device model and said second device model had been configured to closely mimic the logic capabilities of said first one of said plurality of devices and said second one of said plurality of devices respectively, said shareable logic instead being provisioned in said shareable module.** Although, Molero does state modeling a device (server) that contains the ability to generate I/O specific data. The I/O specific data and the method at which it's being created and transmitted is designed to mirror (mimic) the way a physical device (server) would have handled the data (Molero, Page 135, Right Column near center). Still, Molero does not mention that the system contains a shareable module having provisioned shareable logic. However, Ellis mentions a system that contains cache along with the protocol engine (ACS) /(part of a shareable module system) ***the cache [entry] contains a set of initiator parameters such as period, offset, wide/narrow, and speed. In addition to initiator parameters each cache entry also contains a plurality of bits (logic) corresponding to the initiators, which may be supported by the parameters in that cache entry.*** (Ellis, Column 4, Lines 54-59) and the

protocol engine (ACS) connected to the SCSI bus is a master state machine providing the requisite automated logic for sequencing through the SCSI phases and receiving initiator requests. (Ellis, Column 4, Lines 44-48) It would have been obvious to one of ordinary skill to realize that cache entry and the ACS mentioned by Ellis along with the device mirroring (mimicking) described by Molero is functionally equivalent to a shareable module containing shareable logic provisioned to closely mimic the logical capabilities of the devices. The main motivation for combining the teachings of Molero with the teachings of Ellis would be to allow for the support of the ***maximum number of [devices] while minimizing the additional architectural and processing overhead required.*** (Molero, Column 3, Lines 11-13) As a result greater number of devices could be simulated without further expenditure in new system purchases.

As per claim 9, Molero fails to teach **the software-implemented shared bus system model of claim 1 wherein said shareable module further includes I/O-specific access methods.** However, Ellis mentions a system that contains cache along with the protocol engine (ACS) /(part of a shareable module system) ***the cache [entry] contains a set of initiator parameters such as period, offset, wide/narrow, and speed. In addition to initiator parameters each cache entry also contains a plurality of bits (logic) corresponding to the initiators, which may be supported by the parameters in that cache entry.*** (Ellis, Column 4, Lines 54-59) and the ***protocol engine (ACS) connected to the SCSI bus is a master state machine providing the requisite automated logic***

for sequencing through the SCSI phases and receiving initiator requests. (Ellis, Column 4, Lines 44-48) It would have been obvious to one of ordinary skill in the art to realize that the ACS (being part of the shareable module system) contains I/O-specific access methods in form of initiator parameters and logic bits corresponding to the initiators. Therefore, the motivation to combine the teachings of Molero with the teachings of Ellis would be to allow for communication between the shareable module system and the devices.

As per claim 10, Molero fails to teach the ***software-implemented shared bus system model of claim 1 wherein said shareable module further includes functions for configuration of I/O specific parameters.*** However, Ellis mentions a system that contains cache along with the protocol engine (ACS) /(part of a shareable module system) ***the cache [entry] contains a set of initiator parameters such as period, offset, wide/narrow, and speed. In addition to initiator parameters each cache entry also contains a plurality of bits (logic) corresponding to the initiators, which may be supported by the parameters in that cache entry.*** (Ellis, Column 4, Lines 54-59) and the ***protocol engine (ACS) connected to the SCSI bus is a master state machine providing the requisite automated logic for sequencing through the SCSI phases and receiving initiator requests.*** (Ellis, Column 4, Lines 44-48) It would have been obvious to one of ordinary skill in the art that cache [entry] (part of the shareable module) initiator parameters such as "period, offset, wide/narrow, and speed" are functionally equivalent to "functions for configuration

of I/O specific parameters." Therefore the act of configuration of those parameters would require information regarding the data being sent and such information in digital logic can be represented as the period, offset, wide/narrow and the speed of the communication. Therefore, the motivation to combine the teachings of Molero with the teachings of Ellis would be to allow for communication between the shareable module system and the devices by assuring proper I/O configuration.

Claim 13 differs from claims 1,6 and 10 only in statutory basis. Otherwise, the limitations of claim 13 are essentially the same as those of claims 1,6 and 10. Therefore, the limitations of claim 13 are rejected for the same reasons provided in the discussion of claims 1,6 and 10.

Claim 15 states that the protocol monitor module can be expanded to at least one other module whereupon claim 6 states that the protocol monitor module monitors the interactions between the first device model and second device model. Also it is understood that the data to be monitored is shareable data mentioned in claim 13. Consequently, claim 15 differs from claim 6 in statutory basis and enumeration of devices. Otherwise, the limitations of claim 15 are essentially the same as those of claim 6. Therefore, the limitations of claim 15 are rejected for the same reasons provided in the discussion of claim 6.

Claim 16 states that the timing monitor module can be expanded to at least one other module whereupon claim 2 states that the timing monitor module monitors the interactions between the first device model and second device model. Consequently, claim 16 differs from claim 2 in statutory basis and enumeration of devices. Otherwise, the limitations of claim 16 are essentially the same as those of claim 2. Therefore, the limitations of claim 16 are rejected for the same reasons provided in the discussion of claim 2.

The limitations of claim 17, rejected for the same reasons outline in the rejection of claim 1.

The limitations of claim 18, rejected for the same reasons outline in the rejection of claim 2.

The limitations of claim 19, rejected for the same reasons outline in the rejection of claim 3.

The limitations of claim 20, rejected for the same reasons outline in the rejection of claim 4.

The limitations of claim 21, rejected for the same reasons outline in the rejection of claim 7.

The limitations of claim 24, rejected for the same reasons outline in the rejection of claim 6.

The limitations of claim 27, rejected for the same reasons outline in the rejection of claim 9.

The limitations of claim 28, rejected for the same reasons outline in the rejection of claim 10.

3. Claims 5,11,12,14,22,23,25 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***A tool for the Design and Evaluation of Fiber Channel Storage Area Networks*** by Xavier Molero et al. here in "Molero", in view of U.S. Patent 6,112,278 titled ***Method to Store Initiator Information for SCSI Data Transfer*** by Jackson L. Ellis herein "Ellis" and further in view of ***Monitoring Parallel Interfaces in System Environment*** by J. Sosnowski et al. here in "Sosnowski".

As per claim 5, Molero does not teach the **software-implemented shared bus system model of claim 2 wherein said shareable module further includes a timing monitor module, said timing monitor module having access to said first shareable data and said second shareable data to configure, during configuration of said shared bus system model, said timing monitor module to facilitate monitoring of interactions at the timing level, during**

execution, among said first device model, said second device model, and said timing monitor module. However, Sosnowski teaches a system that contains interface-monitoring tool that is capable of distinguishing horizontal decomposition. And ***Horizontal decomposition corresponds to different levels of interface function realization e.g. physical, signal timing...***(Sosnowski, Page 462, Left column near center). An ordinarily skilled artisan would find it obvious to combine the teachings of Molero and Ellis with the teachings of Sosnowski. The motivation for the integration of the teachings would be to ***simplify interface checking, verification, troubleshooting***(Sosnowski, Page 462, left column, bottom) and also allowing for the creation of ***not typical situations in the tested interface [in order] to [provide] the possibility of checking how the interface or coupled devices are capable to recover from these situations. For example reaction of the initiator in SCSI if a target returns more data then requested.***(Sosnowski, Page 463, left column, near center).

As per claim 11, Molero fails to teach ***the software-implemented shared bus system model of claim 1 wherein said shareable module further includes interface to higher level routines.*** However, Sosnowski teaches employing ***higher level analysis...to track data and information flow in the interface.***(Sosnowski, Page 463, Left column near top). It would have been obvious to one of ordinary skill in the art to combine the teachings of Molero and Ellis with the teachings of Sosnowski in order to further test the behavior of the

system in the higher level routines. For example by employing the higher level routines the designer is capable of ***generating erroneous situations in the interface***, ***create strange phase sequences, control service requests***,(Sosnowski, Page 463, Left column near center) allowing the user to test how the ***interface or coupled devices are capable to recover from these situations***. (Sosnowski, Page 463, Left column near center)

As per claim 12, Molero fails to explicitly teach ***the software-implemented shared bus system model of claim 1 wherein said shared bus represents a SCSI (Small Computer System Interface) bus and wherein said shareable logic represents a bus arbitration function.*** However, Ellis teaches that ***to initiate a data transfer process, the initiator causes the bus to enter an "arbitration bus phase." During the arbitration bus phase, each initiator arbitrates for the bus with the other initiators by asserting the appropriate SCSI bus conductor corresponding with a SCSI identifier unique to that specific initiator***(Ellis, Column 2, Lines 16-21). Also Ellis teaches that ***each cache entry also includes a series of bits for locking the cache entry. A handshake from the microprocessor to each arbiter...is provided through the request lock bits.*** (Ellis, Column 4, Lines 65-57 and Column 5, Line 1). It would have been obvious to one of ordinary skill to combine the teachings of Molero with the teachings of Ellis in order to assure that every device on the bus is given the appropriate response in the appropriate amount of time. One way of

achieving that condition would be by employing an arbitrator device, which has been described by Ellis.

Claim 14 states that the timing monitor module can be expanded to at least one other module whereupon claim 5 states that the timing monitor module monitors the interactions between the first device model and second device model. Consequently, claim 14 differs from claim 5 in statutory basis and enumeration of devices. Otherwise, the limitations of claim 14 are essentially the same as those of claim 5. Therefore, the limitations of claim 14 are rejected for the same reasons provided in the discussion of claim 5.

The limitations of claim 22, rejected for the same reasons outline in the rejection of claim 12.

The limitations of claim 23, rejected for the same reasons outline in the rejection of claim 5.

The limitations of claim 25, rejected for the same reasons outline in the rejection of claim 5.

The limitations of claim 29, rejected for the same reasons outline in the rejection of claim 11.

4. Claim 8,26 is rejected under 35 U.S.C. 103(a) as being unpatentable over ***A tool for the Design and Evaluation of Fiber Channel Storage Area Networks*** by Xavier Molero et al. here in "Molero", in view of U.S. Patent 6,112,278 titled ***Method to Store Initiator Information for SCSI Data Transfer*** by Jackson L. Ellis herein "Ellis" and further in view of U.S. Patent 5,825,752 titled ***Local area network transferring data using isochronous and asynchronous channels*** by Fujimori Junichi herein "Junichi".

As per claim 8, Molero fails to teach ***the software-implemented shared bus system model of claim 1 wherein shareable module further includes I/O-specific reset handlers.*** However, Junichi teaches a method of adding extra devices into the bus system by employing I/O reset handlers as a way to reset and reconfigure all logical paths of the bus in order to assigns a new device ID to the newly added device. (Junichi, Column 14, Lines 11-13). It would have been obvious to one of ordinary skill in the art to combine the teachings of Molero and Ellis with the teachings of Junichi in order to arrive at a device bus simulation system that would allow for hot swappable reconfiguration capability. Such capability would allow the user to freely add and remove the bus devices without the necessity to manually reconfigure the simulation as a result allowing for greater flexibility in the design. Finally the employment of reset handlers in a bus system is very well known in the art.

The limitations of claim 26, rejected for the same reasons outline in the rejection of claim 8.

CONCLUSION

Claims 1-29 are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dariusz Basiaga whose telephone number is (571) 272-7133. The examiner can normally be reached on M-F 9:00 – 5:00. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from the either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have

questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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